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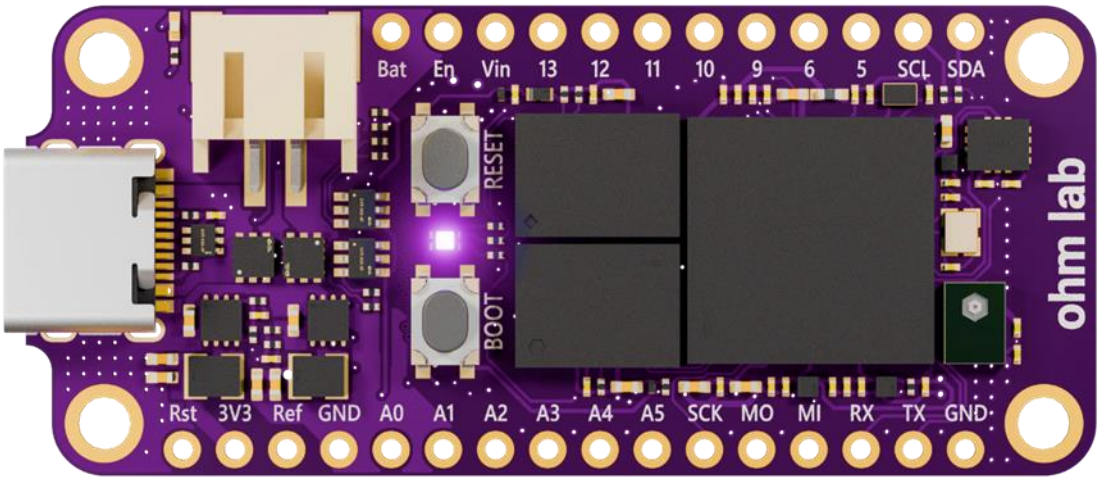
Neuro N6 Development Board

Datasheet

Revision α.01 (Pre-Production)



Overview

- STM32N657I0 Microcontroller
  - Arm® 32-bit Cortex®-M55, 800 MHz
  - ST Neural-ART Accelerator, 600 GOPS
- 4.2 Mbyte contiguous SRAM + 64 Mbyte OctoSPI PSRAM
- 32 Mbyte OctaFlash memory
- Power from USB-C port or single Li-ion Cell with Ideal diode Or-ing, 500mA charging
- Onboard PDM Microphone, IMU, Magnetometer
- Multiple function headers, configurable within software
  - Feather mode: Fully compatible with Adafruit Feather specification
  - Ethernet mode: RMII Ethernet conforming to IEEE 802.3 specification, for use with Neuro ETH expansion board
- One 30 pin and one 40 pin board-to-board connector
  - MIPI CSI-2 interface supporting up to 5MP camera
  - RGB565 LCD interface
  - High speed SDMMC for WIFI or SD card, configurable in software
  - 4 wire UART for BLE connectivity
  - Inter-Integrated Circuit (I2C)
  - Serial Audio Interface (SAI), input or output

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1. Introduction

The Neuro N6 Development Board is a user-friendly and accessible Edge AI development platform featuring an onboard Neural Accelerator. It enables users to explore and experiment with edge AI applications without requiring extensive prior knowledge or experience in artificial intelligence or embedded systems. The capabilities of the Neuro N6 Development Board can be further expanded through compatibility with Ohm Lab's range of Neuro Shields.

The Neuro N6 Arduino core, available at www.ohmlab.co.uk, provides a simplified programming interface via the Arduino IDE. It includes a set of pre-built example applications that allow users to evaluate and experience the board's capabilities immediately after setup. (TBC)

This document describes the features, electrical characteristics, and mechanical specifications of the Neuro N6 Development Board. For instructions on operating and programming the device, please refer to the tutorials available at www.ohmlab.co.uk. (TBC)

For information regarding Neuro Shields, which expand the functionality and capabilities of the Neuro N6 Development Board, please consult the corresponding datasheets available at www.ohmlab.co.uk. (TBC)

For detailed technical information on the STM32N6 Microcontroller, please refer to the official STMicroelectronics datasheet and reference manual RM0484.

Note – Rev α (Pre-Production) datasheet predates all other documentation for the Neuro N6 platform.

2. Features

Table 1: Neuro N6 Features

STM32N657I0 Microcontroller	
Arm® 32-bit Cortex®-M55 core	• 800 MHz frequency • 32 Kbyte ICACHE • 32 Kbyte DCACHE • Arm MVE (M-profile vector extension) • Helium™ technology • TrustZone® MPU
ST Neural-ART Accelerator (Neural processing unit)	• 1 GHz frequency • 600 Billion operations per second (GOPS) • 288 MAC/cycle • Specialized hardware units for DNN (deep-neural network) inference functions • Flexible dedicated stream processing engine • Real-time encryption/decryption • On-the-fly weight decompression
Integrated memory	• 4.2 Mbyte contiguous SRAM • 128 Kbyte TCM (tightly-coupled memory) RAM with ECC for critical real-time data + 64-Kbyte instruction TCM RAM with ECC for critical real-time routines
Graphics	• Neo-Chrom 2.5D GPU: scaling, rotation, alpha blending, texture mapping, perspective transformation • Chrom-ART Accelerator (DMA2D) • Hardware JPEG codec with MJPEG, H.264 encoding • LCD-TFT controller up to XGA resolution
On board sensors	
LSM6DSL Inertial Measurement Unit	• 3D accelerometer with configurable ±2/±4/±8/±16 g range • 3D gyroscope with configurable ±125/±245/±500/±1000/±2000 dps range • Embedded temperature sensor
MP34DT06J Microphone	• Omnidirectional MEMS digital mono microphone (PDM)
MMC5603NJ Magnetometer	• ± 30 Gauss range, 0.0625mG resolution • Enables heading accuracy of ±1°

External Memories	
MX25UM25645G flash memory	• 256 Mbit (32 Mbyte) CMOS serial flash memory • Octo-SPI interface, up to 400Mbit/s data transfer rate and 200MHz clock frequency
IS66WV032M8DALL Random Access Memory (RAM)	• 512Mbit (64 Mbyte) serial PSRAM memory • Octo-SPI interface, up to 400Mbit/s data transfer rate and 200MHz clock frequency
Hardware interfaces	
Header pins (multifunctional)	• Feather mode, fully complies to Adafruit Feather specification – SPI, I2C, UART interfaces – 5 analogue GPIOs, all with ADCs – 7 digital GPIOs, of which 4 PWM capable – Reset, power enable inputs – VBUS, VBAT, 3V3 power and analogue 1V8 reference voltage outputs • Ethernet mode: RMII 10/100 Mbit ethernet interface to external PHY (NeuroETH)
1 x 40 Pin & 1 x 30 Pin board to board connectors	• MIPI CSI-2 camera interface supporting up to 5MP camera • I2C bus • SPI interface • SDMMC 4 bit interface • LTDC (RGB565) LCD screen interface • UART 4 wire interface • Serial Audio Interface (SAI) • SWDIO, SWCLK & NRST • 3V3, 1V8, V_{IN} Power
USB-C connector	• USB High Speed 480Mbit/s Internal PHY
Battery connector	• Supports 3.7V (Single Cell) Li/ion or LiPo battery • On board 500mA charger via USB-C
User interfaces	
LEDs	• User programmable RGB LED • Charging status LED
Buttons	• Reset button • User button

3. Mechanical Dimensions

Table 2*:* Neuro N6 Physical Specifications

Measurement	Value
Size	53.04 x 22.83 x 8.85 mm
Weight	6.7 g

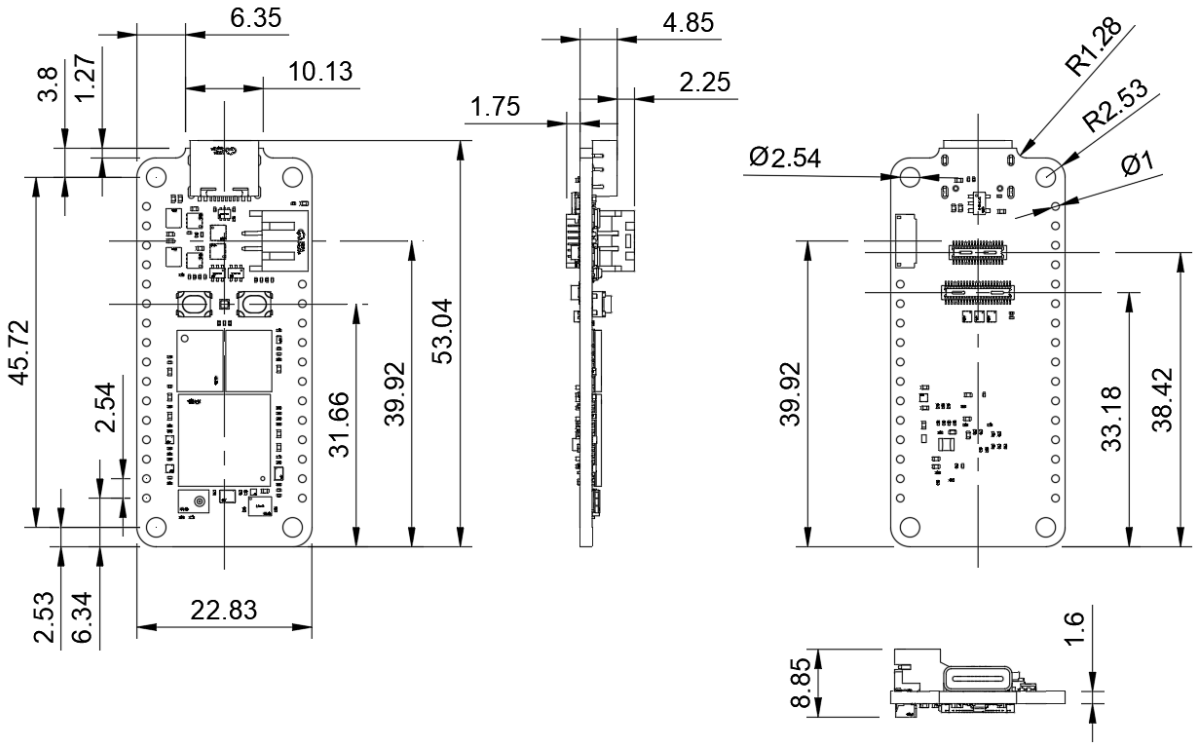

Figure 1: Neuro N6 dimensions

4. Block diagram

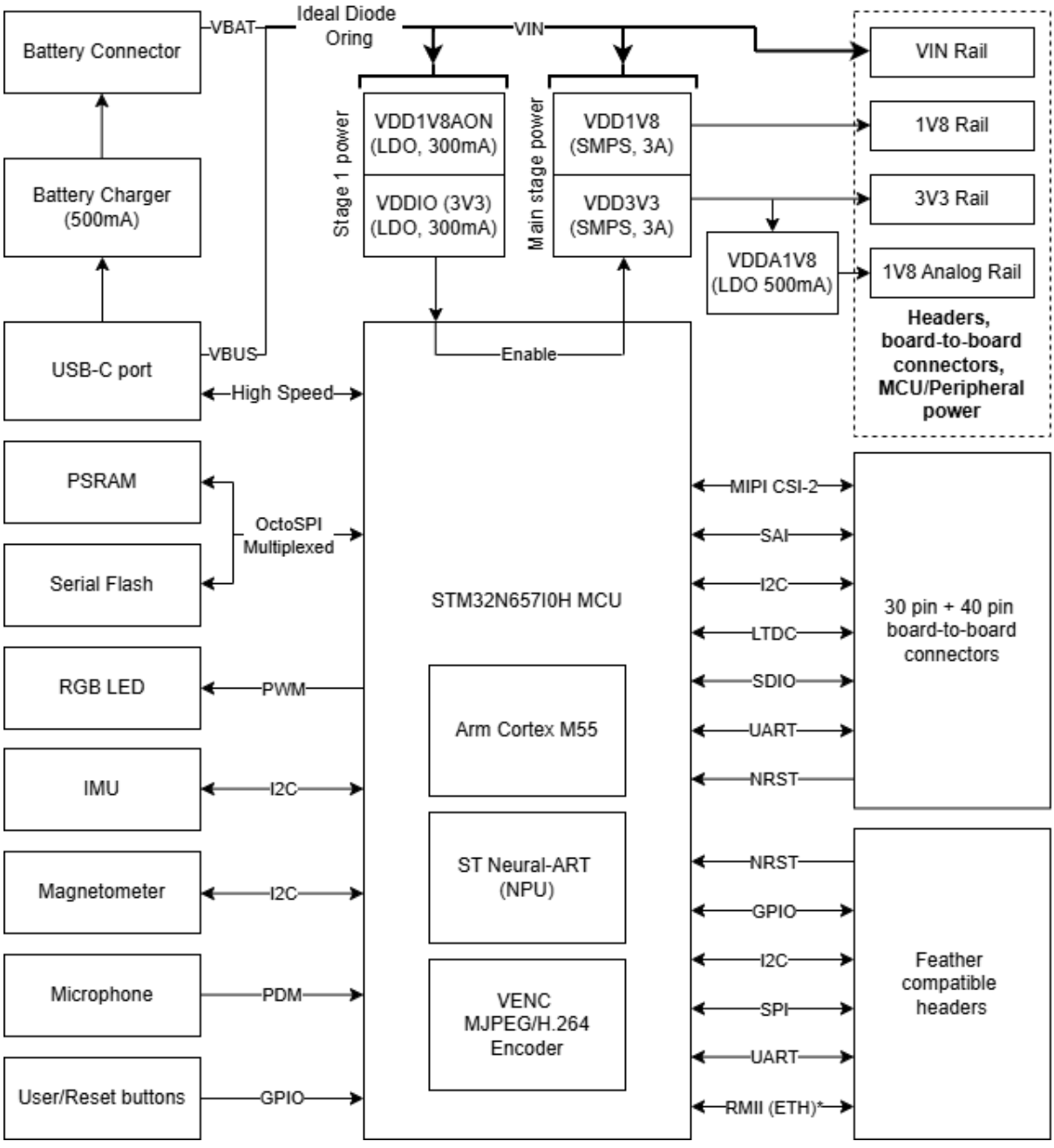

Figure 2: Neuro N6 block diagram

*Configuring ethernet RMII functionality in software disables all primary functions on the header pins.

5. Hardware Interfaces

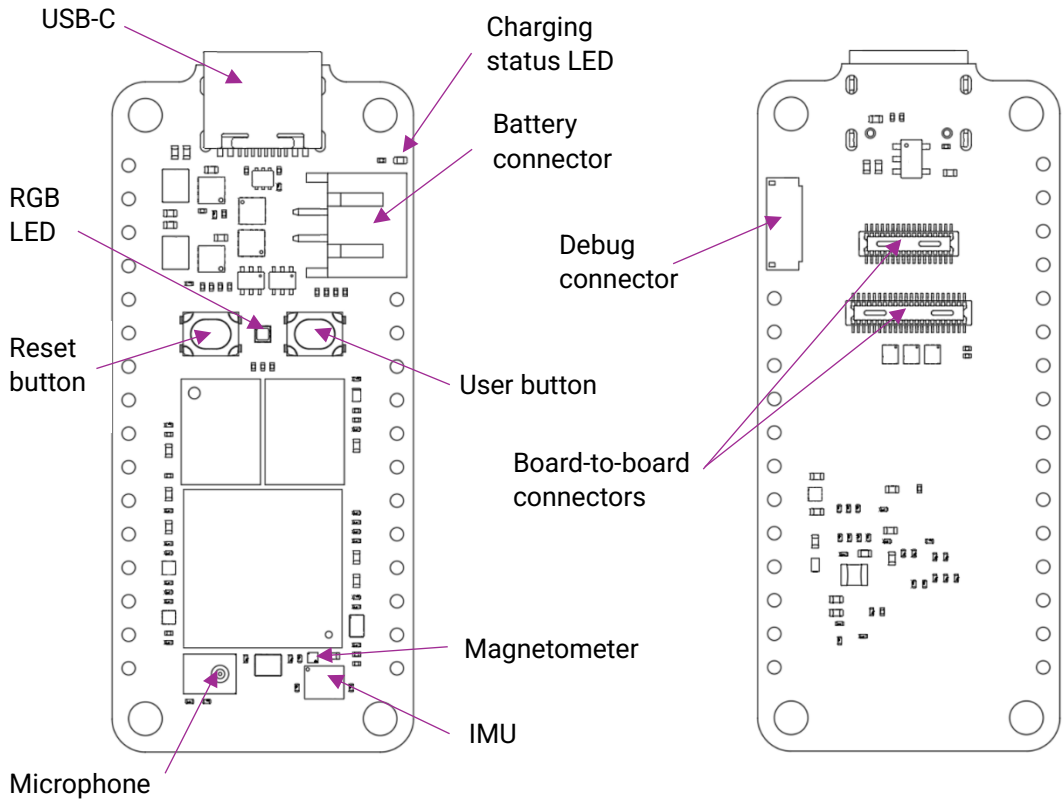

Figure 3: Neuro N6 Hardware Interfaces

5.1 Buttons

The Neuro N6 has two buttons:

- **Reset button:** Performs reset of MCU and peripherals via respective reset pins. Double clicking this button will manually enter the Neuro N6 into bootloader mode: See section 6.4: Boot modes
- **User button:** Programmable GPIO button. Default state is unused.

5.2 LEDs

The Neuro N6 has two LEDs:

- **RGB LED:** Fully user programmable in main application. During bootloader mode, this LED will slowly pulse red.
- **Charging status indicator LED:** Not user programmable. This LED has three states:
    1. **On (Red):** Battery charging
    2. **Flashing 20Hz (Red):** VBUS connected, no battery connected
    3. **Off:** Battery fully charged, or no VBUS connected

5.3 Sensors

The Neuro N6 has three onboard sensors:

- **Inertial Measurement Unit (IMU):** 6 axis IMU with integrated temperature sensor, part number LSM6DSL
- **Magnetometer:** 3 axis magnetometer, part number MMC5603NJ
- **Microphone:** Digital PDM mono microphone, part number MP34DT06J

Please see the respective manufacturer's datasheets for full specifications.

5.4 Connector specifications

Table 3: Connector Specifications

Connector	Part number	Mating part number
Battery connector	S2B-PH-SM4-TB	PHR-2
Debug connector	M0800RS-06-GN	M0800HI-06-GN
30 pin board-to-board connector	HC-PBB40C-30DP-0.4V-02	HC-PBB40C-30DS-0.4V-3.5-02
40 pin board-to-board connector	HC-PBB40C-40DP-0.4V-02	HC-PBB40C-40DS-0.4V-3.5-02

The minimum mating height of the board-to-board connection assembly is 3.5mm. When designing custom expansion boards, this minimum mating height should be respected to allow clearance for manually soldered headers on the Neuro N6. For full pinout of each connector, please refer to the Neuro N6 Schematic (TBC).

5.5 Header pins

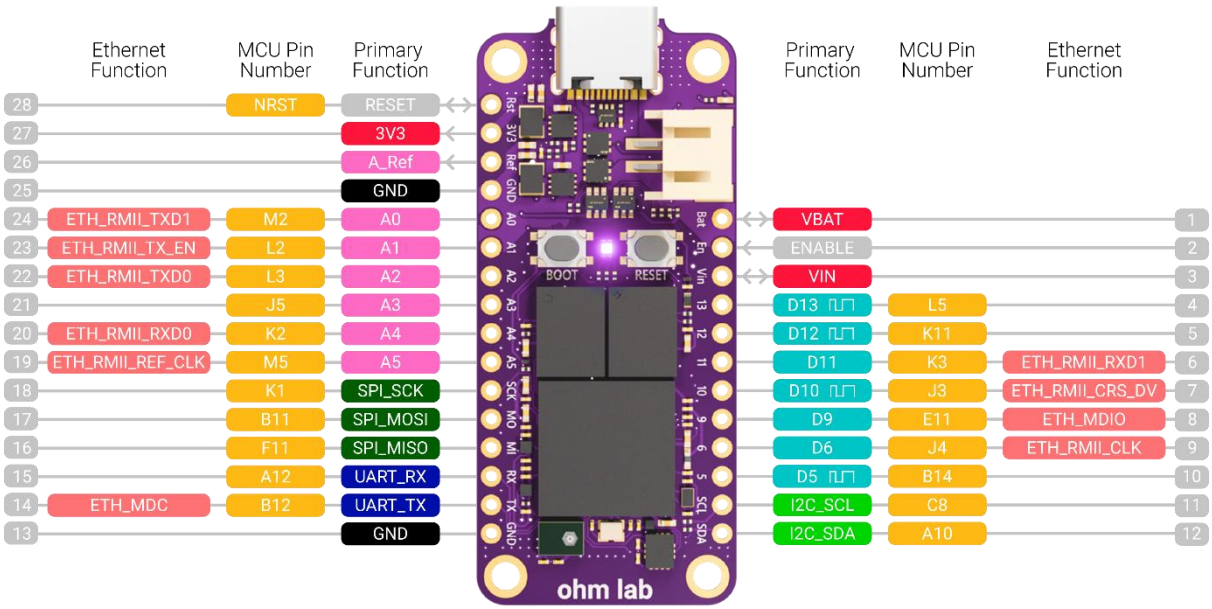

Figure 4: Neuro N6 Header Pin Functions

6. Board operation

6.1 Electrical Characteristics

Table 4: Board electrical characteristics

Parameter	Min	Typical	Max	Unit
Board Supply Voltage (Vbus)	4.5	5	5.5	V
Board Supply Voltage (Vbat)	3.5	3.7	4.3	V
Power consumption during inference*	TBC	750**	TBC	mW
Output voltage (VDD_3V3)	3.2	3.3	3.4	V
Output voltage (VDD_1V8)	1.75	1.8	1.85	V
GPIO voltage range	-0.3	3.3	3.6	V
GPIO current limit	-	-	4	mA

*Neuro N6 + Neuro Vision OV5640, total power consumption

**5V @150mA, measured at VIN pin using 5V bench power supply

Caution: During heavy operation, the board may become warm to the touch, and the linear charger IC may become hot to the touch during battery charging. Initial testing indicates that the Neuro N6 with the Neuro Vision module does not reach temperatures that would cause burns under normal contact; however, appropriate care should still be exercised. Always validate safe operation before deployment.

6.2 Power Supply

The Neuro N6 can be powered by a DC 5V power supply connected to either the USB-C port or VIN pin on the headers or board-to-board connectors. Alternatively, you may power the board with a standard 3.7V single cell Li-ion or LiPo battery. Both a 5V DC supply and 3.7V battery can be connected simultaneously, where this is the case the on-board battery charger will begin charging the battery, and Ideal Diode Or-ing will supply the board power from either supply. You must ensure the power supplied to the board is sufficient for the entire system, see section 6.3 Power Rail Output.

Warning: Do not connect more than one 5V DC supply to the board, for example to the USB-C port and VIN pin simultaneously. This will cause power supply contention and may cause permanent damage to the board or power supplies, fire or serious injury.

Warning: Do not connect any other type of battery other than a **rechargeable 3.7V (single cell) Li-ion or LiPo** battery. Connecting a non-rechargeable battery, or battery with a different voltage level may cause permanent damage to the board or battery, fire or serious injury.

6.3 Power Rail Output

The Neuro N6 can supply power to external expansion boards from 3 separate voltage rails: VIN (Power from battery or USB-C through OR-ing), 3V3 and 1V8. There is also an analogue 1V8 reference voltage with low power supply capability.

Table 5: Power rail supply capability

Voltage Rail	Board consumption	Max supply for external devices	Unit
VDD_3V3	TBD	1000*	mA
VDD_1V8	TBD	1000*	mA
VIN	TBD	1000*	mA
VDDA_1V8 (VREF)	TBD	100	mA

*Limited by calculated thermal performance of traces. Further testing required to confirm exact maximum capability.

Caution: When powering external devices from the voltage rail pins, ensure that either VBAT or VBUS can supply the required power for the entire system. Insufficient power supply may result in voltage drop or brownout and can permanently damage devices connected to affected rails.

Warning: When powering external devices from the voltage rail pins, ensure the total power demand at each rail does not exceed the capability of each rail. Doing so may cause the board to malfunction or overheat, causing fire or serious injury.

6.4 Boot modes

The Neuro N6 has two primary boot modes and two developer boot modes accessed via the boot pins on the debug connector.

6.4.1 Boot from flash

This is the default boot mode on the Neuro N6. The board will load an application file from the external flash into internal RAM and execute.

Due to the way Ohm Lab has configured the STM32N6 internal memory and application boot protocol, the maximum application size is currently 1 Mbyte. This may be increased as development continues.

6.4.2 Ohm Lab OEM Bootloader mode

The Board's application firmware and Neural Network weights can be updated by entering Ohm Lab's OEM Bootloader mode. This allows programming of the external flash using the USB-C port, via Arduino IDE or Ohm Lab's Neuro N6 Uploader software. Bootloader mode is activated in one of two ways:

- Auto-entry: Arduino IDE automatically initiates bootloader mode via the upload button. Any application created in Arduino IDE contains mandatory application code for auto-entry which detects upload button press and initiates a system reset into bootloader mode.
- Manual entry: Manually double-tapping the reset button on the Neuro N6 with a gap of less than 900ms between each press will enter bootloader mode. This function does not require any mandatory application code and can be used to recover the board from a corrupted Arduino application.

Caution: When programming the external flash on board the Neuro N6, do not overwrite the address 0x90000000 – 0x90100000. This area is protected and houses Ohm Lab's OEM First Stage Bootloader (FSBL), which controls both normal boot of application code and Ohm Lab's OEM bootloader mode. Ohm Lab has taken steps to protect this area of the flash memory to prevent accidental corruption of this code, however in the event of corruption or deletion, the board can be recovered using Developer Boot mode, see section 6.4.4.

6.4.3 STMicroelectronics Serial Boot mode

This is a serial boot mode on the STM32N6 entered by asserting the BOOT0 pin on the STM32N6 during a reset or power cycle. It is not recommended to use this mode as Ohm Lab has not implemented a usable protocol using this boot mode.

6.4.4 STMicroelectronics Developer Boot mode

This is the developer boot mode on the STM32N6 entered by asserting the BOOT1 pin on the STM32N6 during a reset or power cycle. This mode allows debugging of the Neuro N6 in STM32 Cube IDE or programming the external flash on the Neuro N6 in STM32 Cube Programmer, using the Neuro N6's external memory loader. With this boot mode it is possible to recover a Neuro N6 following corruption or deletion of Ohm Lab's OEM First Stage Bootloader (FSBL).

For more information on the STM32N6 boot protocol and memory configuration, or Ohm Lab's specific implementation for the Neuro N6, please see the following documentation:

- STM32N6 FSBL explained
- STM32N6 datasheet
- STM32N6 reference manual
- Neuro N6 flash memory configuration - TBC
- How to recover Neuro N6 from FSBL corruption or deletion - TBC

7. Peripheral Interfaces

The following sections outline the STM32N6 peripheral interfaces exposed on board the Neuro N6, including MCU and connector pin numbers and net names. For developers seeking complete connector pinout information to develop custom expansion modules for the Neuro N6, please see the Neuro N6 Schematic - TBC. For detailed information on each of the STM32N6's peripherals, please refer to the STM32N6 datasheet and reference manual.

7.1 MIPI CSI-2

One 2-lane MIPI CSI bus with internal D-PHY compatible with MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.3.

Table 6: MIPI Camera Serial Interface Pin Numbering

Net name	MCU pin number	Connector pin	Description
CSI_D0_P	P4	40DP:10	CSI data lane 0 positive signal
CSI_D0_N	N4	40DP:12	CSI data lane 0 negative signal
CSI_CLK_P	P3	40DP:18	CSI clock lane positive signal
CSI_CLK_N	N3	40DP:20	CSI clock lane negative signal
CSI_D1_P	P2	40DP:26	CSI data lane 1 positive signal
CSI_D1_N	N2	40DP:28	CSI data lane 1 negative signal

7.2 SDMMC

One 4-bit SDMMC interface supporting up to 200MHz clock rate. Can be used for either an SD card slot or to communicate with a wireless module for WI-FI connectivity, configurable in software.

Table 7: SDMMC Pin Numbering

Net name	MCU pin number	Connector pin	Description
SD_CMD	E6	40DP:38	SDMMC command signal
SD_CK	D7	40DP:36	SDMMC clock signal
SD_D0	C6	40DP:33	SDMMC data signal bit 0
SD_D1	D6	40DP:40	SDMMC data signal bit 1
SD_D2	D8	40DP:2	SDMMC data signal bit 2
SD_D3	C7	40DP:34	SDMMC data signal bit 3

7.3 I2C

Two inter-integrated circuit (I2C) interfaces, one exposed on Adafruit Feather header pins and one on 40 pin board to board connector. These buses are shared with sensors on board the Neuro N6 and contain on board pull up resistors, refer to the Neuro N6 schematic (TBC) for more information.

Table 8: Inter-Integrated Circuit Pin Numbering

Net name	MCU pin number	Connector pin	Description
I2C1_SCL	C8	AFH:SCL	I2C1 Clock signal
I2C1_SDA	A10	AFH:SDA	I2C1 Data signal
I2C2_SCL	D12	40DP:6	I2C2 Clock signal
I2C2_SDA	C12	40DP:4	I2C2 Data signal

7.4 SPI

Two Serial Peripheral Interfaces (SPI), one exposed as a secondary function when SDMMC is not being utilised.

Table 9: Serial Peripheral Interface Pin Numbering

Net name	MCU pin number	Connector pin	Description
SPI2_SCK	K1	AFH:SCK	SPI2 Clock signal
SPI2_MISO	F11	AFH:MISO	SPI2 Master in slave out signal
SPI2_MOSI	B11	AFH:MOSI	SPI2 Master out slave in signal
SPI3_SCK*	D8	40DP:2	SPI3 Clock signal
SPI3_MISO*	C7	40DP:34	SPI3 Master in slave out signal
SPI3_MOSI*	D7	40DP:36	SPI3 Master out slave in signal

*Only available when SDMMC is not being utilised. This interface is used by the Neuro Thermal expansion board.

7.5 UART

Two Universal Asynchronous Receiver/Transmitter interfaces. One two-wire interface exposed on the Adafruit Feather headers, and one high speed four-wire interface exposed on the board-to-board connectors, utilised for BLE connectivity on the Neuro expansion boards.

Table 10: Universal Asynchronous Receiver Transmitter Pin Numbering

Net name	MCU pin number	Connector pin	Description
UART4_RX	A12	AFH:RX	UART4 Receive signal
UART4_TX	B12	AFH:TX	UART4 Transmit signal
USART6_RX	A9	30DP:25	USART6 Receive signal
USART6_TX	A8	30DP:27	USART6 Transmit signal
USART6_RTS	B13	30DP:21	USART6 Request to Send signal
USART6_CTS	A13	30DP:24	USART6 Clear to Send signal

7.6 SAI

One Serial Audio Interface (SAI) for I2S PCM Audio output or input. Can be configured in software to either receive PCM Audio from a microphone or transmit PCM audio to a Digital to Analogue Converter (DAC) for speaker output. The B block of the SAI1 peripheral on the STM32N6 is exposed.

Table 11: Serial Audio Interface Pin Numbering

Net name	MCU pin number	Connector pin	Description
SAI1_MCLK_B	N9	30DP:30	SAI1 block B Master clock signal
SAI1_SCK_B	M9	30DP:16	SAI1 block B Serial clock signal
SAI1_FS_B	N11	30DP:4	SAI1 block B Frame select signal
SAI1_SD_B	G13	30DP:14	SAI1 block B Serial data signal

7.7 GPIO

Table 12: Digital GPIO Pin Numbering

Net Name	MCU pin number	Connector pin	Description
D5	B14	AFH:D5	PWM capable digital I/O
D6	J4	AFH:D6	General purpose digital I/O
D9	E11	AFH:D9	General purpose digital I/O
D10	J3	AFH:D10	PWM capable digital I/O
D11	K3	AFH:D11	General purpose digital I/O
D12	K11	AFH:D12	PWM capable digital I/O
D13	L5	AFH:D13	PWM capable digital I/O

Table 13: Analogue GPIO Pin Numbering

Net Name	MCU pin number	Connector pin	Description
A0	M2	AFH:A0	General purpose I/O with ADC
A1	L2	AFH:A1	General purpose I/O with ADC
A2	L3	AFH:A2	General purpose I/O with ADC
A3	J5	AFH:A3	General purpose I/O with ADC
A4	K2	AFH:A4	General purpose I/O with ADC
A5	M5	AFH:A5	General purpose I/O with ADC

7.8 RMII Ethernet

The Adafruit feather header pins may be configured to Reduced Media Independent Interface (RMII) interface to give ethernet connectivity conforming to IEEE 802.3 using the NeuroETH expansion board.

Table 14: Ethernet RMII Pin Numbering

Net Name	MCU pin number	Connector pin	Description
ETH1_RMII_REF_CLK*	M5	AFH:A5	50 MHz reference clock signal
ETH1_CLK*	J4	AFH:D6	Ethernet peripheral clock signal
ETH1_RMII_CRS_DV*	J3	AFH:D10	Carrier Sense / Data Valid signal
ETH1_RMII_RXD0*	K2	AFH:A4	Receive data bit 0 signal
ETH1_RMII_RXD1*	K3	AFH:D11	Receive data bit 1 signal
ETH1_RMII_TX_EN*	L2	AFH:A1	Transmit Enable signal
ETH1_RMII_TXD0*	L3	AFH:A2	Transmit data bit 0 signal
ETH1_RMII_TXD1*	M2	AFH:A0	Transmit data bit 1 signal
ETH1_RMII_MDIO*	E11	AFH:D9	Management Data I/O signal
ETH1_RMII_MDC*	B12	AFH:TX	Management Data Clock signal

*Configuring ethernet RMII functionality in software disables all primary functions on the header pins.

7.9 LTDC Display

The Neuro N6 exposes the LTDC controller on the STM32N6 in 16-bit mode (RGB565) to interface with the Neuro Vision TFT expansion board. For developers wishing to implement custom LCD screen expansion boards, refer to the Neuro N6 Schematic (TBC) for full connector pinout. The LTDC controller supports up to XGA resolution.

8. Document Revision History

Table 15: Document Revision History

Revision	Date	Description
Revision α	15/03/2026	Pre-Production first release
Revision α.01	21/03/2026	Removed 32MB PSRAM option